

CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Canceled)**
2. **(Currently Amended)** The method as claimed in claim ~~1~~ 5, wherein the semiconductor power switch used is an IGBT or MOS power transistor, and the gate terminal and the emitter terminal are connected to one another with high impedance in the case of the intrinsically turned-off IGBT, as a result of which a short-time switch-on of the semiconductor power switch is achieved when a current spike occurs.
3. **(Currently Amended)** The method as claimed in claim ~~1~~ 5, wherein the control terminal of the turned-off semiconductor power switch has applied to it a voltage pulse of predetermined duration and amplitude in a manner temporally coordinated with the occurrence of a current spike at the freewheeling device.
4. **(Currently Amended)** The method as claimed in claim ~~1~~ 5, wherein the control terminal of the turned-off semiconductor power switch has applied to it a stepped voltage pulse of predetermined short time duration in a manner temporally coordinated with the occurrence of a current spike.

5. (Currently Amended) ~~The method as claimed in claim 1,~~ A method for limiting an overvoltage at a freewheeling device arranged in parallel with a semiconductor power switch, wherein at least a first and a second semiconductor power switch are connected in series, each of the first and second semiconductor power switches being parallel-connected with an associated freewheeling device, and an output terminal to an inductive load is arranged between the two, the method comprising the steps of:

- controlling one of the semiconductor power switches into the turned-off state and the other one into the non-turned-off state,

- switching the turned-off semiconductor power switch, at least at the instant of the occurrence of an overvoltage at the associated freewheeling device or during the decay of a current spike, temporarily on to such an extent that a short-time current is generated at the output of the semiconductor power switch;

wherein the voltage at the associated freewheeling device is fed back via a feedback path to an output amplifier stage of a gate driver connected to the control terminal of the turned-off semiconductor power switch, as a result of which the turned-off semiconductor power switch is momentarily and at least partially switched on during the voltage spike.

6. (Currently Amended) ~~The method as claimed in claim 1,~~ A method for limiting an overvoltage at a freewheeling device arranged in parallel with a semiconductor power switch, wherein at least a first and a second semiconductor power switch are connected in series, each of the first and second semiconductor power switches being parallel-connected with an associated freewheeling device, and an output terminal to an inductive load is arranged between the two, the method comprising the steps of:

- controlling one of the semiconductor power switches into the turned-off state and the other one into the non-turned-off state,

- switching the turned-off semiconductor power switch, at least at the instant of the occurrence of an overvoltage at the associated freewheeling device or during the decay of a current spike, temporarily on to such an extent that a short-time current is generated at the output of the semiconductor power switch;

wherein ~~the~~ a current gradient in the freewheeling device is fed back via a further feedback path ~~to the~~ between a control terminal and an emitter terminal of the turned-off semiconductor power switch in such a way that the turned-off semiconductor switch is momentarily and at least partially switched on during the current spike.

7. (Currently Amended) A circuit arrangement for limiting an overvoltage at a freewheeling device arranged in parallel with a semiconductor power switch, comprising at least a first and a second semiconductor power switch each parallel-connected with a freewheeling device being connected in series, an output terminal arranged between the first and second semiconductor power switch for coupling with to an inductive load, and a feedback path between the output of each semiconductor power switch and an amplifier stage of a driver connected to its a control terminal of each power switch.

8. (Original) The circuit arrangement as claimed in claim 7, wherein the feedback path has at least one component, which permits a driving of the control terminal only above a threshold voltage, so that only voltages greater than a predetermined threshold value are fed back to the control terminal.

9. (Original) The circuit arrangement as claimed in claim 7, wherein the feedback path has a component, via which a feedback to the control terminal is effected in a manner proportional to the voltage rise at the freewheeling device.

10. (Original) The circuit arrangement as claimed in claim 7, wherein two zener diodes connected in antiparallel are used as the components in the feedback path.

11. (Original) The circuit arrangement as claimed in claim 7, wherein a capacitor is used as the component in the feedback path.

12. (Original) The circuit arrangement as claimed in claim 7, wherein a parallel circuit comprising zener diodes and an external capacitor is used in the feedback path.

13. **(Currently Amended)** A circuit arrangement for limiting an overvoltage at a freewheeling device arranged in parallel with a semiconductor power switch, comprising at least a first and a second semiconductor power switch each parallel-connected with a freewheeling device being connected in series, an output terminal arranged between the first and second semiconductor power switch for coupling with to an inductive load, wherein a feedback path is provided between the input and control terminal of a power driver, the feedback path being designed such that it permits the control terminal to be driven up only above a threshold value of ~~the~~ a current gradient through the freewheeling device.

14. **(Currently Amended)** The circuit arrangement as claimed in claim 13, wherein ~~the~~ a voltage drop across internal and/or external leakage inductances is utilized for the feedback.

15. **(Currently Amended)** The circuit arrangement as claimed in claim 13, wherein ~~the~~ a current rise is fed back through the induction in a transformer.

16. (Original) The circuit arrangement as claimed in claim 7, wherein an IGBT power transistor is used as the semiconductor power switch.